In the Claims

Please cancel claims 2, 12-29, 34-40, and 45-51.

Please amend the claims as follows:

- 1 1. (Amended) A method of reducing interference in a circuit having a PLL, wherein the
- 2 circuit is formed on an integrated circuit, the method comprising the steps of:
- 3 providing a divider circuit at the input of the PLL for dividing the frequency of an input signal by
- 4 a desired amount; and
- 5 [providing the divider circuit by placing a fixed-value divider at the input of the PLL to reduce
- 6 the digital current created by the PLL.]
- 7. wherein the divider circuit is provided by placing first and second fixed-value dividers connected
- 8 <u>in series at the input of the PLL.</u>
- 1 5. (Amended) A method of reducing interference present in a circuit comprising the step of:
- 2 reducing [the] mutual inductance between digital circuitry in a first portion of the circuit and
- 3 circuitry in a second portion of the circuit by placing a filter between the digital circuitry
- 4 and a voltage source external to the circuit in order to reduce the area of a high frequency
- 5 current loop.
- 1 41. (Amended) A method of reducing interference present in a circuit formed on an
- 2 integrated circuit having PLL and VCO circuitry, the method comprising the step of:

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- [identifying circuitry in the circuit in which the impedance of the circuitry changes state over 3 4 time during operation of the circuit; and] [creating replica circuitry of the identified circuitry which operates in a state opposite of the 5 6 identified circuitry.] creating replica circuitry of first circuitry in the circuit which has an impedance that changes state 7 during operation of the circuit, wherein the replica circuitry operates in an opposite state 8 9 relative to the first circuitry. 1 42. (Amended) The method of claim 41, wherein the [replicated] replica circuitry has no 2 function in the circuit other than reducing interference.
- 43. (Amended) The method of claim 41, wherein the [identified] <u>first</u> circuitry is comprised of a first inverter having a high state and a low state, wherein the replica circuitry is comprised of a second inverter having a high state and a low state, and wherein the [replica] <u>second</u> inverter is controlled to be in the opposite state of the [other] <u>first</u> inverter.
- 44. (Amended) The method of claim 41, wherein the replica circuitry is comprised of circuitry similar to the [identified] <u>first</u> circuitry, the method further comprising the step of connecting an inverter between an input of the [identified] <u>first</u> circuitry and an input of the replica circuitry.

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Please insert the following new claims:

- 1 61. (New) A method of reducing interference present in a circuit formed on an integrated
- 2 circuit, the method comprising the step of:
- 3 providing first circuitry in the circuit, wherein the first circuitry has an impedance that changes
- 4 state during operation of the circuit; and
- 5 creating replica circuitry of the first circuitry, wherein the replica circuitry operates in an opposite
- 6 state relative to the first circuitry.
- 1 62. (New) The method of claim 61, wherein the replica circuitry has no function in the
- 2 circuit other than reducing interference.
- 1 63. (New) The method of claim 61, wherein the first circuitry is comprised of a first inverter
- 2 having a high state and a low state, wherein the replica circuitry is comprised of a second inverter
- 3 having a high state and a low state, and wherein the second inverter is controlled to be in the
- 4 opposite state of the first inverter.
- 1 64. (New) The method of claim 61, wherein the replica circuitry is comprised of circuitry
- 2 similar to the first circuitry, the method further comprising the step of connecting an inverter
- 3 between an input of the first circuitry and an input of the replica circuitry.
- 1 65. (New) The method of claim 61, wherein the integrated circuit has PLL and VCO
- 2 circuitry.

A copy of the pending claims (as amended) is attached.

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